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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/707,486	11/07/2000	Jack D. Pippin	238664US 25 DIV	9610

7590 08/06/2009

R. DANNY HUNTINGTON
BINGHAM MCCUTCHEN, LLP
2020 K STREET, NW
WASHINGTON,, DC 20006

EXAMINER	
FREJD, RUSSELL WARREN	
ART UNIT	**PAPER NUMBER**
2128	

MAIL DATE	DELIVERY MODE
08/06/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/707,486	PIPPIN, JACK D.	
	Examiner	Art Unit	
	Russell Frejd	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 April 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,7-19,22-24,26-30 and 32-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *34* is/are allowed.

6)☒ Claim(s) *1,7-9,11,13,14,16,22-24,26,32,35,37,39 and 40* is/are rejected.

7)☒ Claim(s) *2-4,10,12,17-19,27-30,33,36 and 38* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/30/09; 7/16/09; 7/24/09*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Examination of Application 09/707,486

1. Claims 1-4, 7-19, 22-24, 26-30, and 32-40 of application 09/707,486, filed on 7-November-2000, are pending in the application. Claims 5, 6, 20, 21, 25, and 31 are canceled. The Examiner thanks Applicant for the amendments received to date which have advanced the prosecution of the present application to this point. However, the Examiner is compelled to reopen a previously cited reference, and use this reference as prior art against the claims as cited below.

Claim Rejections under 35 U.S.C. § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2.1 Claims 1, 7-9, 11, 13, 14, 16, 22-24, 26, 32, 35, 37, 39 and 40 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakagawa, Kokai patent Application HEI 2[1990]-83720, published 23-March-1990.

2.2 Nakagawa discloses:

[Claim(s)] 1, 16 and 35: An integrated circuit comprising: a register to store a threshold temperature value [p. 5, lns.21-26, the decoder inherently stores a range of values, including a threshold] ; a thermal sensor [p. 6, ln. 20]; and clock adjustment logic to decrease a clock frequency in response to the thermal sensor indicating that the threshold temperature value has

been exceeded [p. 7, lns. 13-23], the clock adjustment logic further to increase the clock frequency in response to the thermal sensor indicating that the sensed temperature is less than the threshold temperature value [p. 5, lns. 2-5; p. 7, lns. 8-13].

7: a fail-safe sensor [p. 4, ln. 18, see "temperature monitor"] and halt logic to halt operation of the integrated circuit in response to the fail-safe sensor indicating that a fail-safe threshold temperature has been exceeded [p. 4, lns. 2-15].

8: wherein the halt logic comprises logic to inhibit operation of the integrated circuit by stopping a clock of the integrated circuit [p. 4, ln. 4, see "interruptions to processing"].

9: wherein the fail-safe threshold temperature is a predetermined fixed critical temperature [p. 4, lns. 3 "high" and 11 "temperature range", which are both deemed to be inherently predetermined].

11 and 22: an interrupt handler to display information regarding the sensed temperature to a user of the integrated circuit [p. 7, ln. 28, "observed using a program"].

13 and 23: wherein the clock adjustment logic executes instructions to vary the frequency of a clock signal of the integrated circuit in response to the thermal sensor [p. 7, lns. 8-23, see higher frequencies for lower sensed temperatures, and lower frequencies for higher sensed temperatures].

14, 24 and 39: wherein the clock adjustment logic executes instructions to provide closed loop control of the integrated circuit clock frequency, thereby automatically reducing the temperature when overheating occurs [p. 6, ln. 19 “always monitored”; and p. 7, ln. 7 “continuously operated without interruptions”].

26: The limitations of this claim were discussed in the rejection of claims 1, 7 and 8 above, and are therefore considered rejected for the reasons as set forth above. Furthermore, Nakagawa discloses: a programmable thermal sensor [p. 7, lns. 27-29, see “program control”] to receive the register value, wherein the programmable thermal sensor is to generate a first interrupt signal in response to an internal microprocessor temperature exceeding the threshold temperature corresponding to the register value [p. 6, lns. 19-29, see “analog voltage”]; a processor unit coupled to the clock circuitry, wherein the processor unit executes instructions to reduce a frequency of the clock signal in response to the first interrupt signal [p. 7, lns. 13-23].

32: The limitations of this claim were discussed in the rejection of claims 14 and 26 above, and are therefore considered rejected for the reasons as set forth above.

37: The limitations of this claim were discussed in the rejection of claims 7-9 above, and are therefore considered rejected for the reasons as set forth above.

40: programming the microprocessor with a second threshold temperature level [p. 7, lns. 8-13, see the use of a low threshold temperature value.

Claim Rejections under 35 U.S.C. § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in Graham v. John Deere Co., 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering the objective evidence present in the application indicating obviousness or nonobviousness.

3. Claim 15 is rejected under 35 U.S.C. 103 as being unpatentable over Nakagawa, Kokai patent Application HEI 2[1990]-83720, published 23-March-1990, in view of the IBM Technical Disclosure Bulletin, entitled “Automatically Controlled Air Cooling System for Small Machines, dated January 1982.

3.1 Nakagawa does not explicitly disclose interrupt logic to activate an active cooling device in response to the thermal sensor. However, the IBM bulletin discloses air cooling using a fan in response to various threshold temperatures. It would have been obvious to modify the Nakagawa reference to include activating a cooling device to thermally control an electronic circuit in response to a temperature threshold because it would enhance control of the electronic circuit, thereby allowing the electronic circuit to operate at an optimum state.

Claim Objections

4. Claims 2-4, 10, 12, 17-19, 27-30, 33, 36, and 38 are objected to as being dependent upon a rejected base claim, but would be allowable, pending resolution of any rejections noted above, if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The limitations considered allowable are:

[Claim] 2. The integrated circuit of Claim 1 further comprising: threshold adjustment logic to increase the threshold temperature value to a new threshold temperature value in response to the thermal sensor indicating that the threshold temperature value has been exceeded.

3. The integrated circuit of Claim 2 wherein the threshold adjustment logic comprises logic to increase the new threshold temperature value in response to the thermal sensor indicating that the new threshold temperature value has been exceeded.

4. The integrated circuit of Claim 3 wherein the threshold adjustment logic comprises logic to lower the new threshold temperature value to detect decreases in temperature.

10. The integrated circuit of Claim 1 wherein the thermal sensor comprises a plurality of thermal sensors placed across the integrated circuit and an averaging mechanism to calculate an average temperature from the plurality of thermal sensors.

12. The integrated circuit of Claim 10 further comprising: interrupt logic to generate a first interrupt if the calculated average temperature exceeds a first threshold and a second interrupt if the calculated average temperature exceeds a second threshold.

17. The method of Claim 16 further comprising:

increasing the threshold temperature value to a new threshold temperature value in response to the sensed temperature exceeding the threshold temperature value.

18. The method of Claim 17 further comprising increasing the new threshold temperature value in response to the sensed temperature exceeding the threshold temperature value.

19. The method of Claim [[16]] 17 further comprising lowering the new threshold temperature value to detect decreases in temperature.

27. The microprocessor of claim 26 wherein the clock circuitry further comprises a phase locked loop.

28. The microprocessor of claim 26 wherein the thermal sensor comprises: a current source; a voltage reference coupled to the current source to provide a bandgap reference voltage, wherein the bandgap reference voltage is substantially constant over a range of temperatures; programmable circuitry providing an output voltage varying with the microprocessor temperature in accordance with the register value; and a comparator, wherein the comparator generates the first interrupt signal if a difference between the output voltage and the bandgap reference voltage indicates that the threshold temperature has been exceeded.

29. The microprocessor of claim 28 wherein the programmable circuitry further comprises: a transistor coupled to the current source to provide the output voltage, a gain ratio of the output voltage to a junction voltage of the transistor controlled by a transistor bias, wherein the junction voltage varies in accordance with a junction temperature of the transistor, the junction

temperature corresponding to the microprocessor temperature, a bias circuit providing the transistor bias to control the gain ratio, wherein the output voltage varies with the microprocessor temperature in accordance with the register value.

30. The microprocessor of claim 29 wherein the bias circuit further comprises binary weighted resistors.

33. The microprocessor of claim 32 wherein the clock circuitry further comprises: a first clock; a frequency divider coupled to the first clock to provide the clock signal, the frequency divider reducing a frequency of the clock signal in response to the first interrupt signal; and a second clock circuit coupled to provide the clock signal to the microprocessor.

36. The method of claim 35 further comprising: comparing the temperature signal with a second threshold temperature level, wherein the second threshold temperature level represents a fail-safe temperature; and halting the microprocessor, if the temperature signal indicates that the second threshold temperature level has been exceeded.

38. The method of claim 35 wherein generating a temperature signal comprises: providing a bandgap reference voltage, that is substantially constant over a range of temperatures; providing an output voltage varying with the microprocessor temperature in accordance with a stored register value; and wherein generating an interrupt signal comprises generating the ~ interrupt signal if a difference between the output voltage and the bandgap reference voltage indicates that the first threshold temperature level has been exceeded.

Allowed Claims

5. Claim 34 is deemed allowable over the prior art of record at this time, pending resolution of any rejections noted above, because the prior art does not specifically claim the processor unit programming the register with another register value corresponding to another threshold temperature in response to the first interrupt signal.

Response Guidelines

6. A shortened statutory period for response to this action is set to expire **3 (three) months and 0 (zero) days** from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02, 710.02(b)).

6.1 Any response to the Examiner in regard to this non-final action should be

directed to: Russell Frejd, telephone number (571) 272-3779, Monday-Friday from 0530 to 1400 ET, **or** the examiner's supervisor, Kamini Shah, telephone number (571) 272-2279. Inquires of a general nature or relating to the status of this application should be directed to the TC2100 Group Receptionist (571) 272-2100.

mailed to: Commissioner of Patents and Trademarks
P.O. Box 1450, Alexandria, VA 22313-1450

or faxed to: (571) 273-8300

Hand-delivered responses should be brought to the Customer Service Window, Randolph Building, 401 Dulany Street, Alexandria, VA, 22314.

/Russell Frejd/
Primary Examiner AU 2128